



# **JFLEX™-3COMGPIOPCcard-USB** **JFLEX™-4COMGPIOPCcard**

## **Product Manual**

**Document Revision 1.0**

## Table of Contents

<b>JFLEX™-3COMGPIOPCCARD-USB , JFLEX™-4COMGPIOPCCARD.....</b>	<b>I</b>
<b>1 USER INFORMATION .....</b>	<b>3</b>
1.1 ABOUT THIS MANUAL.....	3
1.2 JUMPTEC® BRAND .....	3
1.3 COPYRIGHT NOTICE .....	3
1.4 TRADEMARKS .....	3
1.5 STANDARDS .....	4
1.6 WARRANTY .....	4
1.7 TECHNICAL SUPPORT .....	5
<b>2 INTRODUCTION.....</b>	<b>6</b>
2.1 JFLEX-3COMGPIOPCCARD-USB .....	6
<b>3 SPECIFICATIONS.....</b>	<b>7</b>
3.1 MECHANICAL SPECIFICATIONS.....	7
3.2 ELECTRICAL SPECIFICATIONS.....	9
3.2.1 Supply Voltage.....	9
3.2.2 Supply Voltage Ripple.....	9
1.1.1 Supply Current.....	9
3.3 ENVIRONMENTAL SPECIFICATIONS .....	9
3.3.1 Temperature.....	9
3.3.2 Humidity.....	9
<b>4 MODULE FUNCTIONS .....</b>	<b>10</b>
4.1 COM PORTS A, B, C, D.....	10
4.1.1 Programming .....	10
4.1.2 Connectors.....	10
4.1.3 Connector Pinouts .....	11
4.2 4 X 8-BIT GPIO PORTS .....	12
4.2.1 Programming using 32-Bit Operating Systems.....	12
4.2.2 Programming using 16-Bit Operating Systems.....	12
4.2.3 Connector.....	16
4.2.4 Connector Pinout.....	16
4.3 USB INTERFACE .....	17
4.3.1 General description .....	17
4.3.2 Connector Pinout.....	17
4.3.3 Connector.....	17
4.4 PCMCIA INTERFACE.....	18
4.4.1 Controller.....	18
4.4.2 PC Card Socket Power Interface.....	18
4.4.3 Interrupt Configurations.....	18
4.4.4 Software Considerations.....	19
<b>5 APPENDIX A: BLOCK DIAGRAM.....</b>	<b>20</b>
<b>6 APPENDIX B: LITERATURE AND STANDARDS.....</b>	<b>21</b>
6.1 BUSES AND GENERAL PC ARCHITECTURE .....	21
6.1.1 PCI.....	21
6.1.2 USB.....	21

6.1.3 AC '97..... 21

6.1.4 LPC..... 22

6.2 RS232C, RS485..... 22

**7 APPENDIX C: DOCUMENT REVISION HISTORY ..... 22**

# 1 USER INFORMATION

## 1.1 About This Manual

This document provides information about products from Kontron Embedded Computers AG and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied.

While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied "as-is" and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility.

## 1.2 JUMPt<sup>®</sup> Brand

JUMPt<sup>®</sup> Industrielle Computertechnik AG and Kontron Embedded Computers AG merged in July 2002. JUMPt<sup>®</sup> is now known as Kontron Embedded Modules GmbH.

Products labeled and sold under the Kontron Embedded Modules name (formerly JUMPt<sup>®</sup>) are now considered Kontron products for all practical purposes, including warranty and support.

JFLEX<sup>™</sup>, DIMM-PC<sup>®</sup>, PISA<sup>®</sup>, ETX Components SBC<sup>™</sup>, JUMPt<sup>®</sup>, and Kontron Embedded Modules are trademarks or registered trademarks of Kontron Embedded Modules GmbH.

## 1.3 Copyright Notice

Copyright © 2004 Kontron Embedded Computers AG.

All rights reserved. No part of this manual may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means (electronic, mechanical, photocopying, recording, or otherwise), without the express written permission of Kontron.

## 1.4 Trademarks

The following lists the trademarks of components used in this board.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.

- Microsoft is a registered trademark of Microsoft Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

## 1.5 Standards

Kontron Embedded Modules is certified to ISO 9000 standards.

## 1.6 Warranty

This Kontron Embedded Modules product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

You may receive a bill for test costs if Kontron Embedded Modules finds no fault with the product. You also may receive a bill for repairs if a product's warranty has expired.

For warranty service or repair, return the product to a Kontron Embedded Modules service facility listed in the Technical Support section of this document.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules that are caused by a faulty Kontron Embedded Modules product.

## 1.7 Technical Support

Technicians and engineers from Kontron Embedded Modules and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems. Before contacting Kontron Embedded Modules technical support, please consult our [Web site](#) for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by email or telephone. The table below lists technical support contacts and service facilities for Kontron Embedded Modules.

Asia	Europe	North/South America
<b>Kontron Asia</b>	<b>Kontron Embedded Modules</b>	<b>Kontron Americas</b>
5F-1, 341, Sec 4 Chung Hsiao E. Road Taipei, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	3988 Trust Way Hayward, CA 94545
Tel: +886 2 2751 7192	Tel: +49 (0) 991-37024-0	Tel: 510-732-6900
Fax: +886 2 2772 0314	Fax: +49 (0) 991-37024-104	Fax: 510-732-7655
<a href="http://www.jumptec.com.tw/">http://www.jumptec.com.tw/</a> <a href="http://www.kontron.com.tw/">http://www.kontron.com.tw/</a>	<a href="http://www.jumptec.de/">http://www.jumptec.de/</a> <a href="http://www.kontron-em.de/">http://www.kontron-em.de/</a>	<a href="http://www.adastra.com/">http://www.adastra.com/</a> <a href="http://www.kontron.com/">http://www.kontron.com/</a>
		<a href="mailto:techsupport@jumptec.com">techsupport@jumptec.com</a>

## 2 INTRODUCTION

### 2.1 JFLEX-3COMGPIOPCcard-USB

The JFLEX-4COMGPIOPCcard and JFLEX-3COMGPIOPCcard-USB are extension boards for Kontron's JReX 3,5" embedded line SBC family.

Following features are provided by the 3COMGPIOPCcard-USB

- 3 serial ports RS232 (optional TTL-Level signals)
- 4 x 8-bit GPIO pins
- 2 USB ports
- PCMCIA Ports with PCI1520 Controller:
  - ◆ Two Type I/II or one Type III PC Card or CardBus slots with hot insertion removal
  - ◆ Mix-and-match 5V/3.3V, 16-bit PC Cards and 32-bit CardBus cards
  - ◆ Burst transfers to maximize data throughput with CardBus cards
  - ◆ Intel 82365SL-DF and 82365SL register compatible
  - ◆ Exchangeable Card Architecture (ExCA)
  - ◆ PC Card Standard 1997 16/32-bit 5V/3,3V, PCMCIA /PC Card R2 (16 bit)
  - ◆ PCMCIA /PC Card R2 (16 bit)
  - ◆ Card Bus (32 bit)

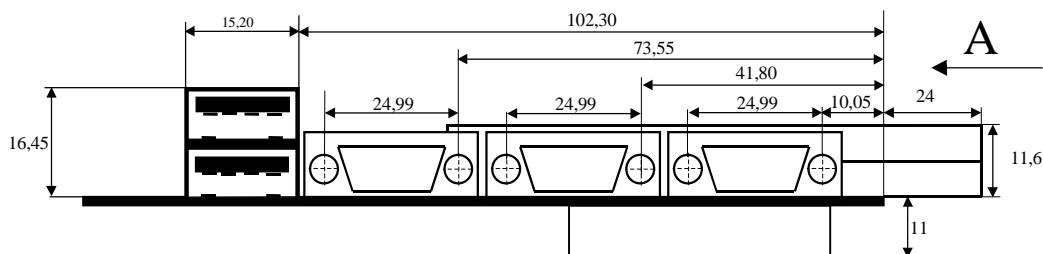
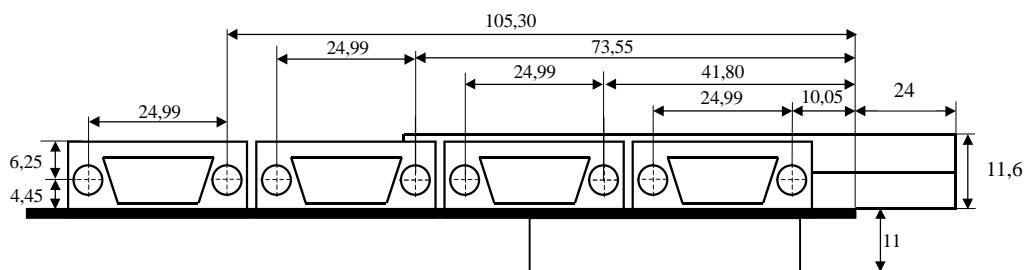
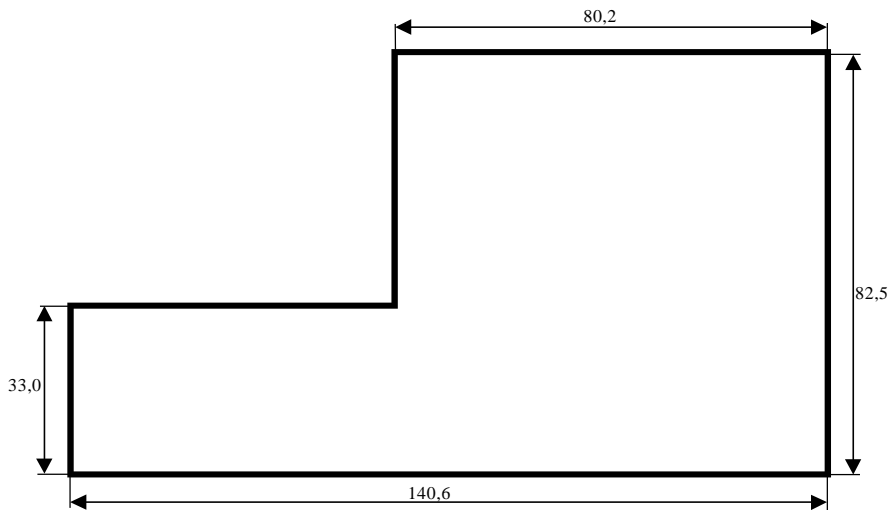
Following features are provided by the 4COMGPIOPCcard

- 3 serial ports RS232 (optional TTL-Level signals)
- 4 x 8-bit GPIO pins
- 1 serial port RS422/RS485
- PCMCIA Ports with PCI1520 Controller:
  - ◆ Two Type I/II or one Type III PC Card or CardBus slots with hot insertion removal
  - ◆ Mix-and-match 5V/3.3V, 16-bit PC Cards and 32-bit CardBus cards
  - ◆ Burst transfers to maximize data throughput with CardBus cards
  - ◆ Intel 82365SL-DF and 82365SL register compatible
  - ◆ Exchangeable Card Architecture (ExCA)
  - ◆ PC Card Standard 1997 16/32-bit 5V/3,3V, PCMCIA /PC Card R2 (16 bit)
  - ◆ PCMCIA /PC Card R2 (16 bit)
  - ◆ Card Bus (32 bit)

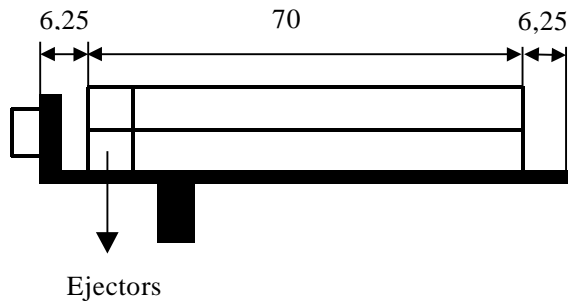
# 3 SPECIFICATIONS

## 3.1 Mechanical Specifications

- Mechanical: PCB 140,6mm x 82,5mm L-shape



A:



All dimensions are given in Millimeters [mm].

## 3.2 Electrical Specifications

### 3.2.1 Supply Voltage

- 5V DC +/- 5%
- 3,3V DC +/- 5%

### 3.2.2 Supply Voltage Ripple

- 100 mV peak to peak 0-20 MHz

### 1.1.1 Supply Current

- @ 3.3V           max. 50mA (without PC-cards)
- @ 5V             max. 200mA

## 3.3 Environmental Specifications

### 3.3.1 Temperature

- Operating: 0 to + 60°C
- Storage: -10 to + 85 ° C

### 3.3.2 Humidity

- Operating: 10% to 90% (non condensing)
- Storage: 5% to 95% (non condensing)

**To protect the external powerlines to peripheral devices the customer has to take care about:**

- **The wires to the external device have the right diameter to withstand the max. available current.**
- **The housing of the external device fulfills the fire protecting requirements of IEC/EN 60950.**

## 4 MODULE FUNCTIONS

### 4.1 COM Ports A, B, C, D

The JFLEX-4COMGPIOPCcard has four 16550-compatible serial ports:

- COM-A
- COM-B
- COM-C
- COM-D

Line drivers used for COM-A through COM-C conform to the IEEE RS-232C standard. COM-D can be selected by jumper to work as RS422 transmitter or RS485 (default). RS485 can be 2-wire or 4-wire system.

COM-D is not available on JFLEX-3COMGPIOPCcard-USB.

#### 4.1.1 Programming

When connected to a JReX CPU module the COM ports can be activated and configured within the systems BIOS setup menu.

The configuration table can be found on I/O Device Configuration screen in the Advanced menu.

*Note: The option "IrDA" in BIOS setup menu is not applicable to JFLEX-4COMGPIOPCCARD and JFLEX-3COMGPIOPCCARD-USB.*

*Do not enable this option for COM operation.*

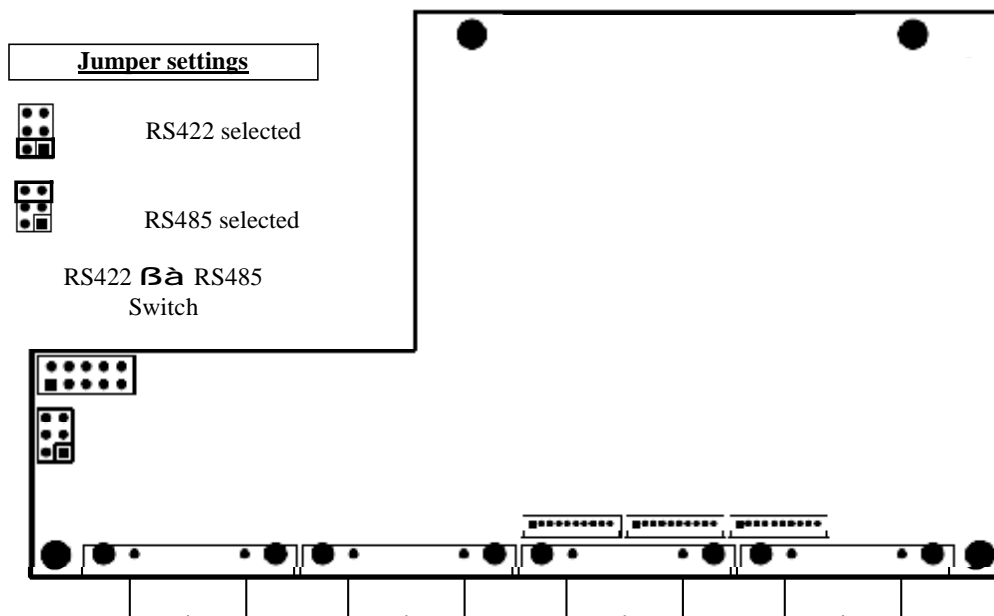
#### 4.1.2 Connectors

COM-A and COM-B have an external DSUB-9 connector to connect RS232 devices and an internal Micro-Header which provides TTL-level COM signal.

RS232 devices at COM-C can either be connected to the DSUB-9 connector at the front or internally at the Micor-Header.

COM-D can be connected to an RS485 (or RS422) network either through the DSUB-9 connector at the front or the internal 10-pin header.

Only one device can be connected at an individual port at one time.



### 4.1.3 Connector Pinouts

COM-A, B, C (RS232 & TTL)				COM-D (RS422 / RS485)			
Signalname	Direction	Pin Header	DSUB-9	Signalname	Direction	Pin Header	DSUB-9
RLSD (A, B, C)	In	1	1	TXD+	Out	1	1
DSR (A, B, C)	In	2	6	RXD+ / TXD+	In / Out	2	6
SIN (A, B, C)	In	3	2	--	--	3	--
RTS (A, B, C)	Out	4	7	--	--	4	--
SOUT (A, B, C)	Out	5	3	TXD-	Out	5	3
CTS (A, B, C)	In	6	8	RXD- / TXD-	In / Out	6	8
DTR (A, B, C)	Out	7	4	--	--	7	--
RI (A, B, C)	In	8	9	--	--	8	--
GND	--	9	5	GND	--	9	5
VCC5	--	10	--	VCC5	--	10	--

For signal description please refer to additional literature.

## 4.2 4 x 8-bit GPIO Ports

The JFLEX-4COMGPIOPCCARD and JFLEX-3COMGPIOPCCARD-USB Modules provide 32 GPIO Pins arranged as 4 x 8-bit ports. Each pin is individually configurable as an input or Open-Drain output. When configured as output the user must provide a pullup resistor to the desired output voltage level. All output pins have 12mA drive strength. The output LowLevel is max. 0,4V.

### 4.2.1 Programming using 32-Bit Operating Systems

Also all GPIO pins can be read or written using JIDA32 protected mode functions. Additional information on how to use JIDA32 and sample code can be found on the Kontron web page at [www.kontron-em.de](http://www.kontron-em.de) and [www.kontron.com](http://www.kontron.com).

### 4.2.2 Programming using 16-Bit Operating Systems

The W83697uf Super I/O controller consists of several logical devices, which correspond to individual functionality. Logical Device 9 reflect the GPIOs 2-4 and Logical Device 8 reflect the GPIO 5. Each Logical Device has it's own configuration registers. The designer can access the desired configuration Registers by selecting a logical device through the Extended Functions Data Register (I/O port index address 4Eh and data address 4Fh).

#### *Configuration Register Logical Device 9 (GPIO 2-4)*

Index F0h: GPIO2 selection register. Default 0FFh  
Index F3h: GPIO3 selection register. Default 0FFh  
Index F6h: GPIO4 selection register. Default 0FFh  
When set to a '1' respective GPIO pin is programmed as an input port  
When set to a '0' respective GPIO pin is programmed as an output port

Index F1h: GPIO2 data register. Default 00h  
Index F4h: GPIO3 data register. Default 00h  
Index F7h: GPIO4 data register. Default 00h  
If GPIO is programmed to be an output port, then the respective bit can be written, else if the GPIO is programmed as input port, then the respective bit can be read.

*Configuration Register Logical Device 8 (GPIO 5)*

Index F0h: GPIO5 selection register. Default 0FFh  
 When set to a '1' respective GPIO pin is programmed as an input port  
 When set to a '0' respective GPIO pin is programmed as an output port

Index F1h: GPIO5 data register. Default 00h  
 If GPIO is programmed to be an output port, then the respective bit can be written, else if the GPIO is programmed to be an input port, then the respective bit can be read.

*Programming example for GPIO3*

```

W83697_IOBASE      EQU      04Eh      ;base address for index/data port
W83697_CONFIG_ENABLE EQU      087h      ;data for unlock sequence
W83697_CONFIG_DISABLE EQU      0Aah      ;data for lock sequence

;+-----
;
; sioGpio3ReadData - read data from GPIO3
;
;   Entry:
;   None
;   Exit:
;   AH: input value
;
sioGpio3ReadData   PROC NEAR PUBLIC
    pushf          ; no INTs while accessing
    cli           ; W83697UF devices.

    Mov    al, 07h      ; device selection register 07h
    mov    ah, 09h      ; select logical device
    call   sioRegWrite8 ;(GPIO port 2-4).

    Mov    al, 0F3h     ; GPIO3 selection register
    mov    ah, 0FFh     ; set to be an input port
    call   sioRegWrite8

    mov    al, 0F4h     ; GPIO3 data register
    call   sioRegRead8  ; read data from port

    popf
    ret
sioGpio3ReadData   ENDP

;+-----
;
; sioGpio3WriteData - write data to GPIO3;
;   Entry:
;   AH: output value
;   Exit:
;   None
;
sioGpio3WriteData  PROC NEAR PUBLIC
    push  ax          ; store output value

```

```

    pushf                ; no INTs while accessing
    cli                  ; W83697UF devices.

    Mov    al, 07h        ; device selection register 07h
    mov    ah, 09h        ; select logical device 9
    call   sioRegWrite8   ;(GPIO port 2-4).

    Mov    al, 0F3h       ; GPIO3 selection register
    mov    ah, 000h       ; set to be an output port
    call   sioRegWrite8

    pop    ax             ; restore output value
    mov    al, 0F4h       ; GPIO3 data register
    call   sioRegWrite8   ; write data to port

    popf
    pop    ax
    ret
sioGpio3ReadData      ENDP

;-----
;
;      sioRegRead8 - reads an 8-bit SIO configuration register
;
;      Entry:
;      AL - register index
;
;      Exit:
;      AH - register value
;
sioRegRead8          PROC NEAR PUBLIC
    pushf                ; no INTs while SIO configuration
    cli                  ; register access.
    Push   dx

    mov    ah, al         ; save register index.

    Mov    dx, W83697_IOBASE ; port 4Fh - perform unlock mechanism.
    Mov    al, W83697_CONFIG_ENABLE
    out    dx, al
    out    dx, al

    mov    al, ah         ; write register index.
    Out    dx, al
    xchg   ah, al

    inc    dx             ; port 4Fh - read register data .
    in     al, dx
    xchg   ah, al

    push   ax             ; Save index and data.

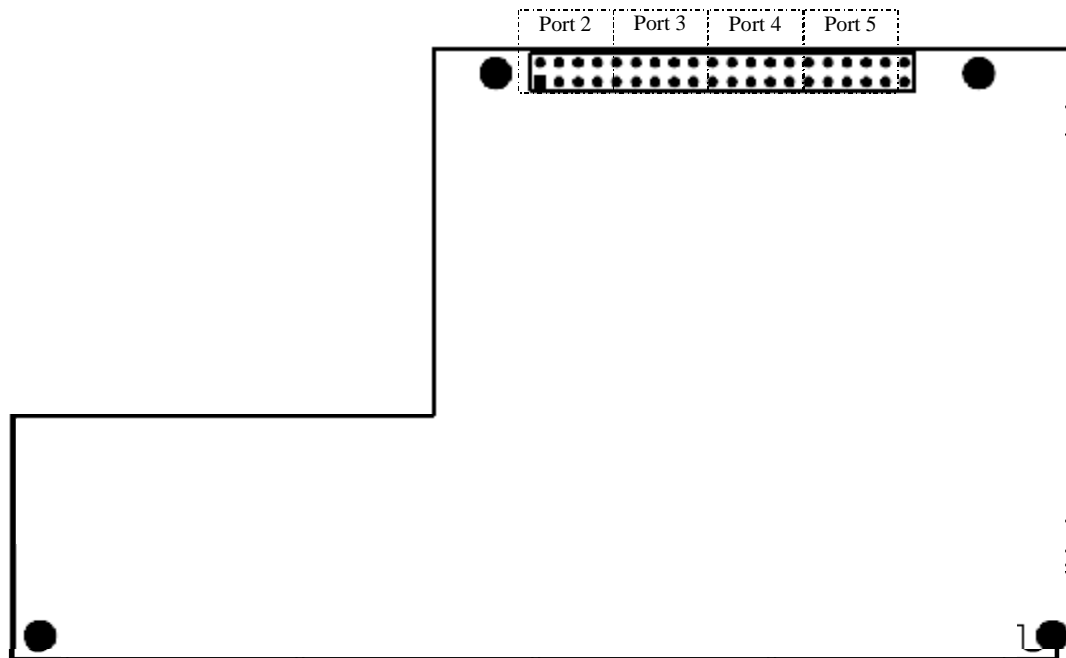
    Dec    dx             ; port 4Eh - perform lock mechanism.
    Mov    al, W83697_CONFIG_DISABLE
    out    dx, al

    pop    ax
    pop    dx
    popf
    ret
sioRegRead8          ENDP

```

```
-----  
;  
;  
;   sioRegWrite8 - writes an 8-bit SIO configuration register  
;  
;   Entry:  
;   AL - register index  
;   AH - register value  
;  
;   Exit:  
;   none  
;  
sioRegWrite8   PROC NEAR PUBLIC  
    pushf                ; no INTs while SIO2 configuration  
    cli                 ; register access.  
    Push  dx  
    push  ax  
  
    mov  dx, W83697_IOBASE    ; port 4Eh - perform unlock mechanism.  
    Mov  al, W83697_CONFIG_ENABLE  
    out  dx, al  
    out  dx, al  
  
    pop  ax                ; port 4Eh - write register index.  
    Push  ax  
    out  dx, al  
  
    mov  al, ah            ; port 4Fh - write register data.  
    Inc  dx  
    out  dx, al  
  
    dec  dx                ; port 4Eh - perform lock mechanism.  
    Mov  al, W83697_CONFIG_DISABLE  
    out  dx, al  
  
    pop  ax  
    pop  dx  
    popf  
    ret  
sioRegWrite8   ENDP
```

### 4.2.3 Connector



### 4.2.4 Connector Pinout

GPIO Port 2		GPIO Port 3		GPIO Port 4		GPIO Port 5	
Pin Nr.	Pin Name	Pin Nr.	Pin Name	Pin Nr.	Pin Name	Pin Nr.	Pin Name
1	GND	11	GND	21	GND	31	GND
2	VCC5	12	VCC5	22	VCC5	32	VCC5
3	GPIO_20	13	GPIO_30	23	GPIO_40	33	GPIO_50
4	GPIO_21	14	GPIO_31	24	GPIO_41	34	GPIO_51
5	GPIO_22	15	GPIO_32	25	GPIO_42	35	GPIO_52
6	GPIO_23	16	GPIO_33	26	GPIO_43	36	GPIO_53
7	GPIO_24	17	GPIO_34	27	GPIO_44	37	GPIO_54
8	GPIO_25	18	GPIO_35	28	GPIO_45	38	GPIO_55
9	GPIO_26	19	GPIO_36	29	GPIO_46	39	GPIO_56
10	GPIO_27	20	GPIO_37	30	GPIO_47	40	GPIO_57

## 4.3 USB Interface

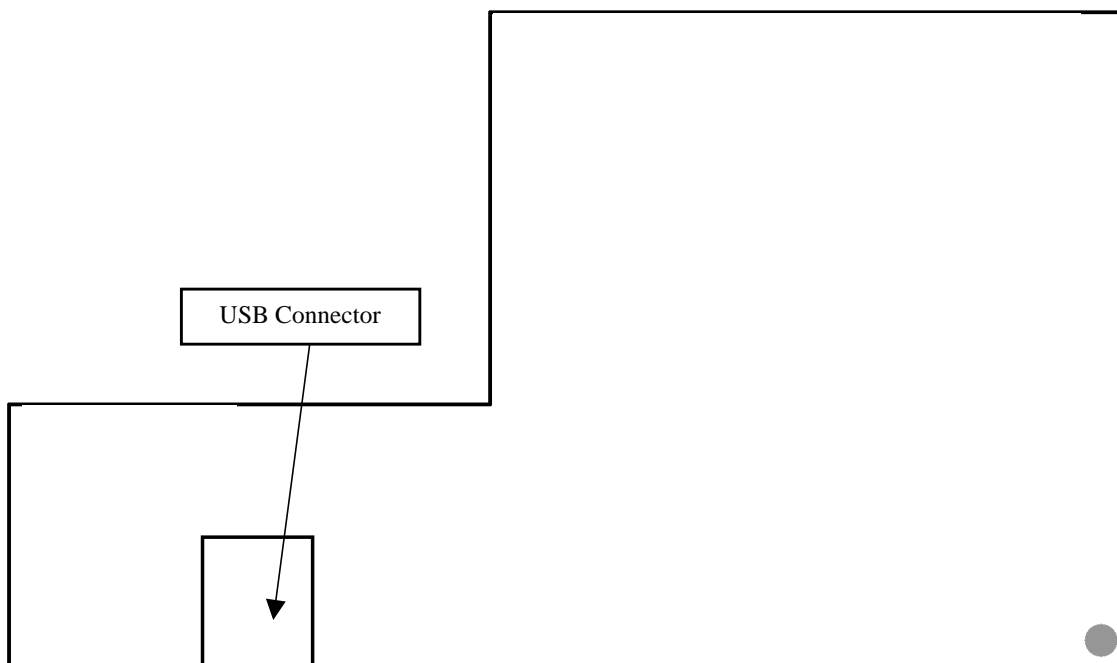
### 4.3.1 General description

The JFLEX-3COMGPIOPCCARD-USB supports two USB ports. You can expand the USB ports by adding external hubs up to an amount of 127 USB peripherals per port.

### 4.3.2 Connector Pinout

Pin	Function
1	USB1_+5V
2	USB1-
3	USB1+
4	USB1_GND
5	USB2_+5V
6	USB2-
7	USB2+
8	USB2_GND

### 4.3.3 Connector



## 4.4 PCMCIA Interface

### 4.4.1 Controller

The Texas Instruments PCI1520 controller features:

- Two PC Card or CardBus slots with hot insertion removal
- Mix-and-match 5V/3.3V, 16-bit PC Cards and 32-bit CardBus cards
- Burst transfers to maximize data throughput with CardBus cards
- Intel 82365SL-DF and 82365SL register compatible
- Exchangeable Card Architecture (ExCA)

### 4.4.2 PC Card Socket Power Interface

The JFLEX-4COMGPIOPCcard and JFLEX-3COMGPIOPCcard-USB modules offer the following power interface features for a PC Card socket:

- Texas Instruments TPS 2223
- +5V/3,3V 1A for each socket
- Short-circuit and thermal protection

### 4.4.3 Interrupt Configurations

CardBus Cards need a PCI interrupt, which is available on INTA# and INTB# on the PCI bus.

For many legacy 16-bit PC cards, a legacy ISA interrupt is required for the card to function properly. Kontron recommends reserving IRQ10 and IRQ11 in the following BIOS submenu of the JFlex board. These interrupts are available for the JFlex connector on the JFlex board.

Using the PhoenixBIOS, go to Setup Utility->PCI Configuration->PCI/PNP ISA IRQ Resource Exclusion Submenu. The submenu is shown below

Feature	Option	Description
IRQ3	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ4	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ5	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ7	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ9	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ10	<b>Reserved</b>	Reserves specified IRQ for use by legacy ISA PCMCIA devices.
IRQ11	<b>Reserved</b>	Reserves specified IRQ for use by legacy ISA PCMCIA devices.
IRQ12	Available	Reserves specified IRQ for use by legacy ISA devices.
IRQ14	Available	Reserves specified IRQ for use by legacy ISA devices. (Visible if primary IDE disabled).
IRQ15	Available	Reserves specified IRQ for use by legacy ISA devices. (Visible if secondary IDE disabled).

#### 4.4.4 Software Considerations

Windows XP supports JFLEX-4COMGPIOPCcard and JFLEX-3COMGPIOPCcard-USB modules. Windows 2000, Windows ME and Windows 98SE will recognize the module as a generic CardBus controller. The device functions properly using these drivers. For many legacy 16-bit PC cards, it is necessary to assign a suitable ISA interrupt in the BIOS setup and the operating system.

Kontron does not support other operating systems. However, many non-Microsoft operating systems have generic CardBus device drivers, which are compatible with the Texas Instruments' PCI1520 cardbus controller or the Intel 82365SL controller.

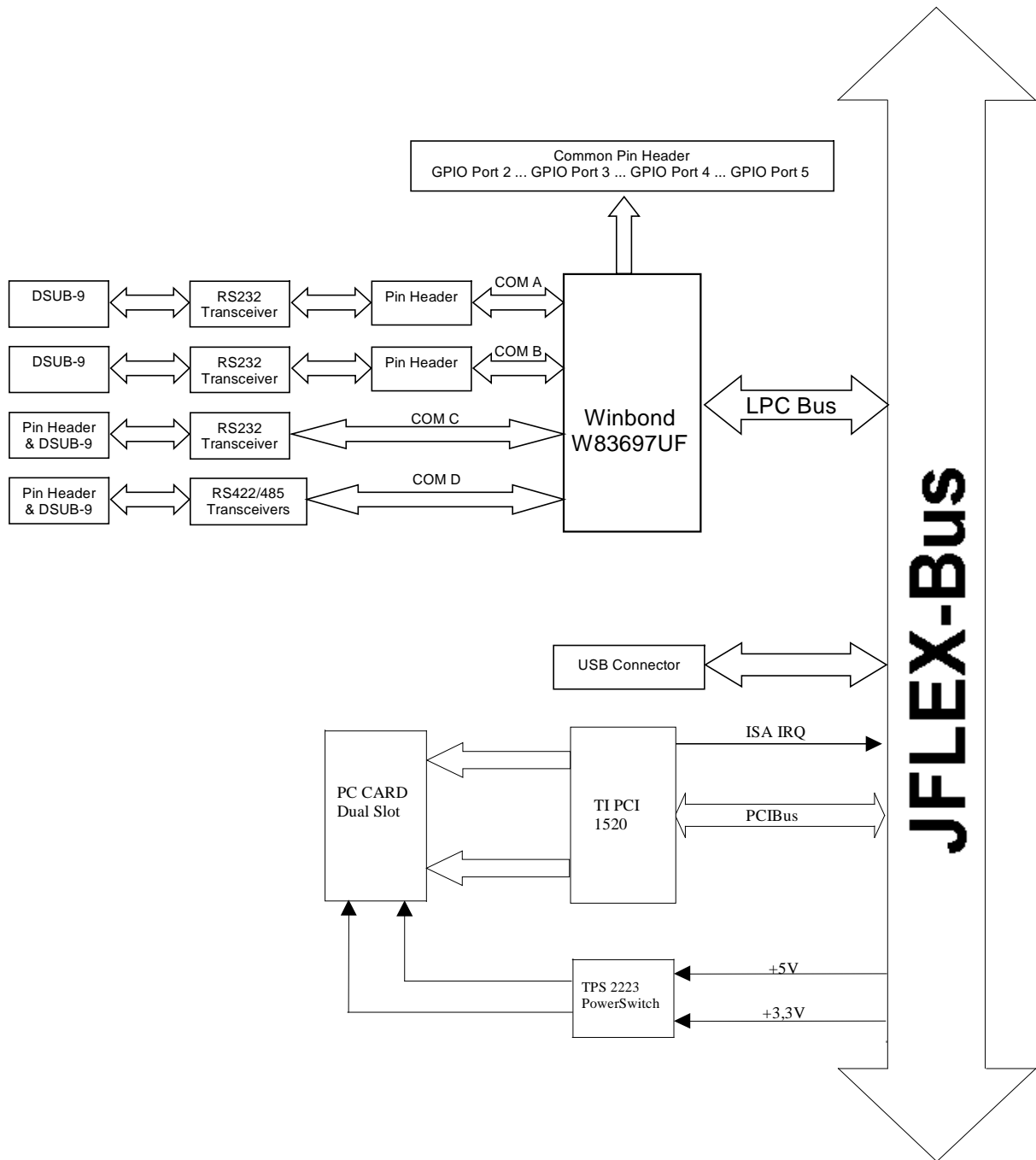
---

Note:

**Windows NT 4.0 only supports 5V legacy 16-bit PC cards. Also, hot-swapping functions are not supported. To drive 3.3V legacy 16-bit PC cards and enable hot-swapping, please use the additional software CardWizardNT, released by SystemSoft. The software is not free.**

---

# 5 APPENDIX A: BLOCK DIAGRAM



## 6 APPENDIX B: LITERATURE AND STANDARDS

Below is a list of information sources to help you to further understand PC architecture.

### 6.1 Buses and General PC Architecture

#### 6.1.1 PCI

PCI spec. @ <http://www.pcisig.com/home/>

- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture*, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

#### 6.1.2 USB

USB spec. @ <http://www.usb.org/>

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology.

#### 6.1.3 AC '97

AC '97 spec. @ <http://www.intel.com/labs/media/audio/>

The specification defines the Audio Codec '97 (AC '97) Architecture and Digital Interface (AC-link) specifically designed for implementing audio and modem I/O functionality in PC systems. This specification does not explicitly define the companion AC '97 Digital Controller component (sometimes referred to or abbreviated as DC '97), which typically varies in features and implementation, but is AC '97 compliant with this specification.

### 6.1.4 LPC

LPC spec. @ <http://www.intel.com/design/chipsets/industry/lpc.htm>

The Low Pin Count (LPC) Interface Specification for legacy I/O has facilitated the industry's transition toward ISA-less systems.

The LPC Interface allows the legacy I/O motherboard components, typically integrated in a Super I/O chip, to migrate from the ISA/X-bus to the LPC Interface, while retaining full software compatibility. The LPC Specification offers several key advantages over ISA/X-bus, such as reduced pin count for easier, more cost-effective design. The LPC Interface Specification is software transparent for I/O functions and compatible with existing peripheral devices and applications.

The LPC Interface Specification describes memory, I/O and DMA transactions. Unlike ISA, which runs at 8MHz, it will use the PCI 33MHz clock and will be compatible with more advanced silicon processes.

## 6.2 RS232C, RS485

- EIA-232-E Interface between data terminal equipment and data circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)
- National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at <http://www.national.com/>. A search engine is provided to search the text of the available application notes. Entering „232“ as search criteria to get a current list of related application notes.
- The link [www.rs485.com](http://www.rs485.com) provides detailed information about RS485 and RS422 interfaces.

## 7 APPENDIX C: DOCUMENT REVISION HISTORY

Version	Date	Edited by	Changes
0.9	04.08.2004	BAJ	First draft
1.0	09.08.2004	BAJ	First public release